OIPE JUL 10 2006 PATENT & TRADEMARK OFFICE

PATENT

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:
SARVAR PATEL
ZULFIKAR AMIN RAMZAN

Examiner: V. Perungavoor

Serial No.: 09/175,178

Group Art Unit: 2132

Filed: OCTOBER 20, 1998

Att'y Docket: 2100.001100

For: EFFICIENT HASHING METHOD

APPEAL BRIEF

CERTIFICATE OF MAILING
37 C.F.R. 1.8

I hereby certify that this correspondence is being deposited with the U.S. Postal Service with sufficient postage as First Class Mail in an envelope addressed to: Assistant Commissioner for Patents, Washington, D.C. 20231, on the date below:

7-5-06
Date

Nancy Nolan
Signature

MAIL STOP APPEAL BRIEF- PATENTS
Commissioner of Patents
P. O. Box 1450
Alexandria, VA 22313-1450

Sir:

Applicants hereby submit this Appeal Brief to the Board of Patent Appeals and Interferences in response to the final Office Action dated February 17, 2006. A Notice of Appeal was filed on May 17, 2006. The statutory response date to file this Appeal Brief is July 17, 2006. This Appeal Brief is being filed on July 5, 2006, therefore, it is timely filed.

If an extension of time is required to enable this paper to be timely filed and there is no separate Petition for Extension of Time filed herewith, this paper is to be construed as also constituting a Petition for Extension of Time Under 37 CFR § 1.136(a) for a period of time sufficient to enable this document to be timely filed.

07/21/2006 SSANDARA 00000003 500786 09175178
01 FC:1402 500.00 DA

A fee in the amount of $500.00 is due as a result of this filing. The Commissioner is authorized to deduct said fee from Williams, Morgan & Amerson, P.C. Deposit Account No. 50-0786/2100.001100. No other fee(s) is believed to be due, however, should any fee(s) under 37 C.F.R. §§ 1.16 TO 1.21 be required for any reason, the Commissioner is authorized to deduct said fee(s) from Williams, Morgan & Amerson, P.C. Deposit Account No. 50-786/2100.001100.

Respectfully submitted,

Date: 7/5/06

Mark W. Sincell, Ph.D.
Reg. No. 52,226
WILLIAMS, MORGAN & AMERSON
10333 Richmond, Suite 1100
Houston, Texas 77042
(713) 934-7000
(713) 934-7011 (facsimile)

AGENT FOR APPLICANTS

I. REAL PARTY IN INTEREST

The present application is owned by Lucent Technologies, Inc. The assignment of the present application to Lucent Technologies, Inc., is recorded at Reel 9682, Frame 0577.

II. RELATED APPEALS AND INTERFERENCES

Applicant is not aware of any related appeals and/or interferences that might affect the outcome of this proceeding.

III. STATUS OF THE CLAIMS

Claims 1-3 are pending in the present application. Claims 1-3 stand rejected under 35 U.S.C. § 101 as being directed to non-statutory subject matter. Claims 1-3 were rejected under 35 U.S.C. § 102(b) as allegedly being anticipated by the Schenier publication.

IV. STATUS OF AMENDMENTS

There were no amendments after the final rejections.

V. SUMMARY OF CLAIMED SUBJECT MATTER

Independent claims 1-3 set forth inputting a collection of "n" bits and producing a shortened representation of the collection of bits. Independent claims 1-3 also set forth summing a key having at least "n" bits with the collection of bits to produce a sum, squaring the sum to produce a squared sum, and performing a modular "p" operation on the squared sum, where "p" is a first prime number greater than 2^n to produce a modular "p" result. Independent claims 2-3 further set forth repeating the summing and squaring steps one or more times to form a

summation of a plurality of squared sums and performing the modular "p" operation on the summation. Independent claims 1-3 then set forth performing a modular 2^l operation on the modular "p" result to produce a modular 2^l result (where "l" is less than "n") and outputting the modular 2^l result. Exemplary embodiments of the inventions set forth in claims 1-3 are described between lines 18 on page 5 and a line 14 on page 7 of the Patent Application. These embodiments are illustrated in Figures 1-3.

VI. GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

Appellant respectfully requests that the Board review and overturn the two rejections present in this case. The following issues are presented on appeal in this case:

(A) Whether claims 1-2 are directed to statutory subject matter; and

(B) Whether claims 1-3 are anticipated by the Schenier publication.

VII. ARGUMENT

A. Legal Standards

An anticipating reference by definition must disclose every limitation of the rejected claim in the same relationship to one another as set forth in the claim. *In re Bond*, 15 U.S.P.Q.2d 1566, 1567 (Fed. Cir. 1990).

B. Claims 1-2 are directed to statutory subject matter.

Section 101 of title 35, United States Code, provides:

Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefore, subject to the conditions and requirements of this title.

The Examiner noted in the Final Office Action that a process that merely manipulates and abstract idea or performs a purely mathematical algorithm may be non-statutory despite the fact that it might inherently have some usefulness. However, in the context of computer-related processes, the MPEP also states that a claimed process is statutory subject matter if it is limited to a practical application of an abstract idea or mathematical algorithm in the technological arts. See MPEP §2106 IV.B.2.b.ii.

Claims 1-3 each set forth inputting a collection of bits and then applying one of the claimed hashing algorithms to the collection of bits to form a hashed collection of bits that is a shortened representation of the collection of bits. The result is then output, *e.g.*, as the output modular 2^l result. Thus, Applicants respectfully submit that claims 1-3 are limited to the practical application of applying the claimed hashing algorithm to a collection of bits to produce a shortened representation of the collection of bits. Embodiments of the inventions set forth in claims 1-3 are also useful. Hashing algorithms such as set forth in claims 1-3 have wide application in a variety of fields. For example, the claimed method may be used to simplify searches for text strings by hashing bits representative of the text strings to reduce the size of the stored information. For another example, the claimed method may be used in various wireless communication applications to shorten the collection of bits that represent an authentication message to a smaller collection of bits that is conventionally referred to as a tag. See Patent Application, pages 2-3.

For at least the aforementioned reasons, Applicants respectfully submit that the invention set forth in claims 1-3 represents a useful practical application in the technological arts and is therefore statutory subject matter. Applicants request that the Examiner's rejections of claims 1-3 under 35 U.S.C. § 101 be REVERSED.

C. **Claims 1-3 are not anticipated by the Schenier publication.**

The Schenier publication describes Jueneman's methods, which teach forming a hash function by applying a mod-p operation, where p is a prime less than 2^m-1. In contrast, claims 1-3 set forth performing a mod-p operation, where *p* is at least as large as a first prime number greater than 2^n. The Schenier publication also describes an IBC hash, which teaches forming a hash function by applying a mod-p operation to a message M, where p is an n-bit prime number. However, the IBC hash fails to teach or suggest performing a mod-p operation on a squared sum, where *p* is at least as large as a first prime number greater than 2^n. Thus, the Schenier publication does not disclose every limitation of the rejected claim in the same relationship to one another as set forth in the claim.

In the Final Office Action, the Examiner admits that the Schenier publication fails to teach or suggest performing a mod-p operation, where *p* is at least as large as a first prime number greater than 2^n. Nevertheless, the Examiner alleges that claims 1-3 are anticipated by the Schenier publication because the specification does not state that using a different range of values of *p* for the mod-p operation would be a major improvement over the range described by the Schenier publication. Applicants respectfully submit that whether or not the ranges set forth in claims 1-3 represent an improvement over the range is described in the Schenier publication is immaterial to determining whether or not the Schenier publication anticipates claims 1-3. As stated above, an anticipating reference by definition *must* disclose every limitation of the rejected claim *in the same relationship to one another* as set forth in the claim. The Schenier publication fails this test and therefore does not anticipate claims 1-3.

For at least the aforementioned reasons, Applicants respectfully submit that the present invention is not anticipated by Schenier publication and request that the Examiner's rejections of claims 1-3 under 35 U.S.C. § 102(b) be REVERSED.

VIII. CLAIMS APPENDIX

The claims that are the subject of the present appeal – claims 1-3 – are set forth in the attached "Claims Appendix."

IX. EVIDENCE APPENDIX

There is no separate Evidence Appendix for this appeal.

X. RELATED PROCEEDINGS APPENDIX

There is no Related Proceedings Appendix for this appeal.

In view of the foregoing, it is respectfully submitted that the Examiner erred in not allowing all claims pending in the present application, claims 1-3, over the prior art of record. The undersigned may be contacted at (713) 934-4052 with respect to any questions, comments or suggestions relating to this appeal.

OIPE JUL 10 2006 PATENT & TRADEMARK OFFICE

CLAIMS APPENDIX

1. (Original) A method for producing a shortened representation of a collection of bits, comprising the steps of:

inputting the collection of "n" bits;

summing a key having at least "n" bits with the collection of bits to produce a sum;

squaring the sum to produce a squared sum;

performing a modular "p" operation on the squared sum, where "p" is a first prime number greater than 2^n to produce a modular "p" result;

performing a modular 2^l operation on the modular "p" result to produce a modular 2^l result where, "l" is less than "n"; and

outputting the modular 2^l result.

2. (Original) A method for producing a shortened representation of a collection of bits, comprising the steps of:

inputting the collection of "n" bits;

summing a first key having at least "n" bits with the collection of bits to produce a first sum;

squaring the first sum to produce a squared sum;

summing the squared sum with a second key having at least "n" bits to produce a second sum;

performing a modular "p" operation on the second sum, where "p" is a first prime number greater than 2^n to produce a modular "p" result;

performing a modular 2^1 operation on the modular "p" result to produce a modular 2^1 result where, "1" is less than "n"; and

outputting the modular 2^1 result.

3. (Original) A method for producing a shortened representation of a collection of bits, comprising the steps of:

inputting a collection of "n" bits;

summing a key having at least "n" bits with the collection of bits to produce a sum;

squaring the sum to produce a squared sum;

repeating the previous three steps at least once to produce a plurality of squared sums, where a different key is used each time the steps are repeated;

summing the plurality of squared sums to produce a summation;

performing a modular "p" operation on the summation, where "p" is a first prime number greater than 2^n to produce a modular "p" result;

performing a modular 2^1 operation on the modular "p" result to produce a modular 2^1 result where, "1" is less than "n"; and

outputting the modular 2^1 result.